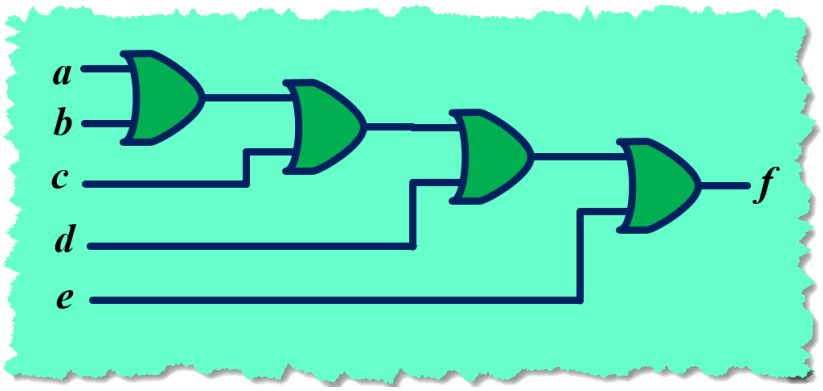
The following graph represents the function before synthesis. It consists of four gates scheduled in four levels.



If we synthesis the code for performance (which is the default assumption in Vivado-HLS), then the following graph represents the function. It consists of four gates organised into three levels.