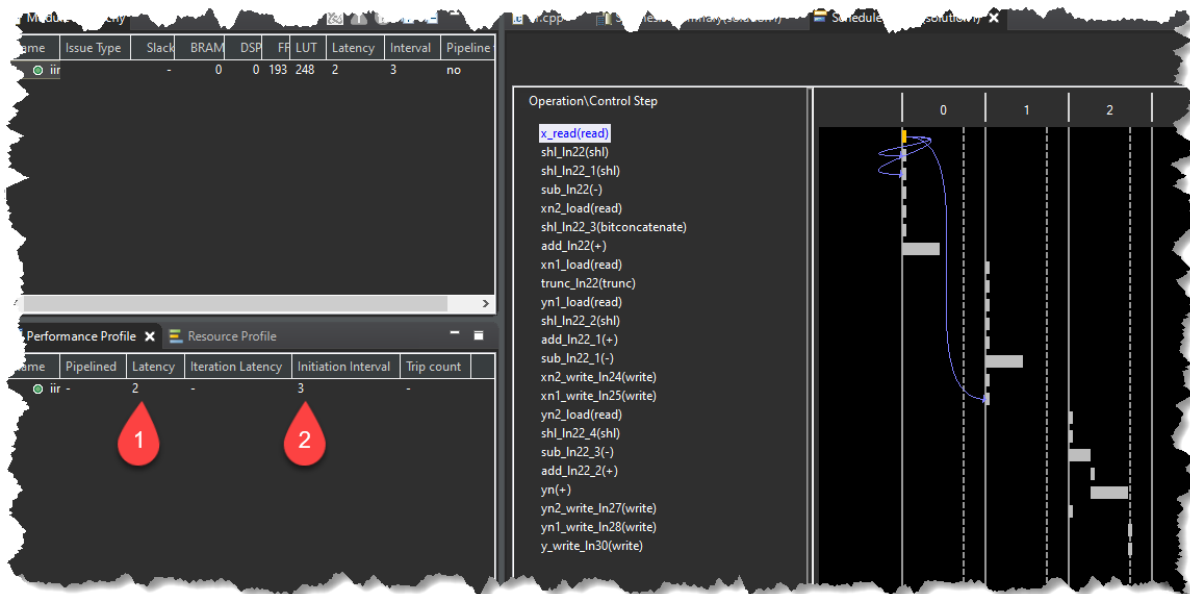


# 1 Digital System Design with High-Level Synthesis for FPGA

## Sequential Circuits

The following figure shows the analysis perspective after high-level synthesis for the non-pipelined IIR design.

As can be seen, the design latency is 2, and the initiation interval is 3. This means the circuit can accept new input every three clock cycles and generate the corresponding output after two clock cycles. Note that in the clock cycle, after generating the output and accepting the new input, the circuit modifies its state registers.



The following figure shows the corresponding timing diagram. In the p1 stage, the circuit accepts new inputs, and in the p2 stage, it generates its output. Therefore, every three clock cycles, the circuit accept a new input which is 32 bits and generate an output which means 32 bits.

Therefore, if the clock frequency is 100 MHz, then the throughput would be

$$\frac{32 \text{ bit}}{3 * 10ns} = 133.3 \text{ MByte/s}$$

